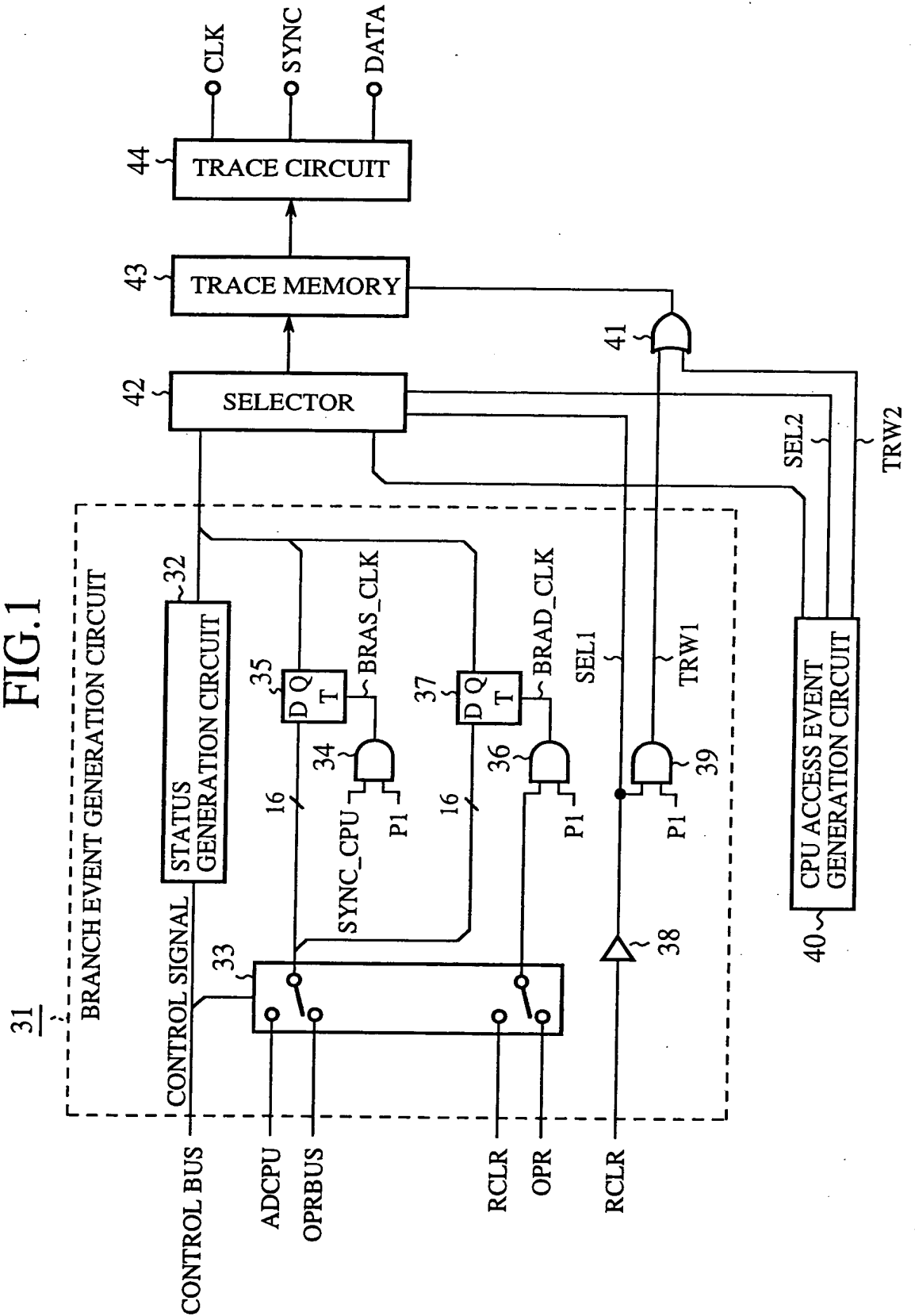


FIG.1



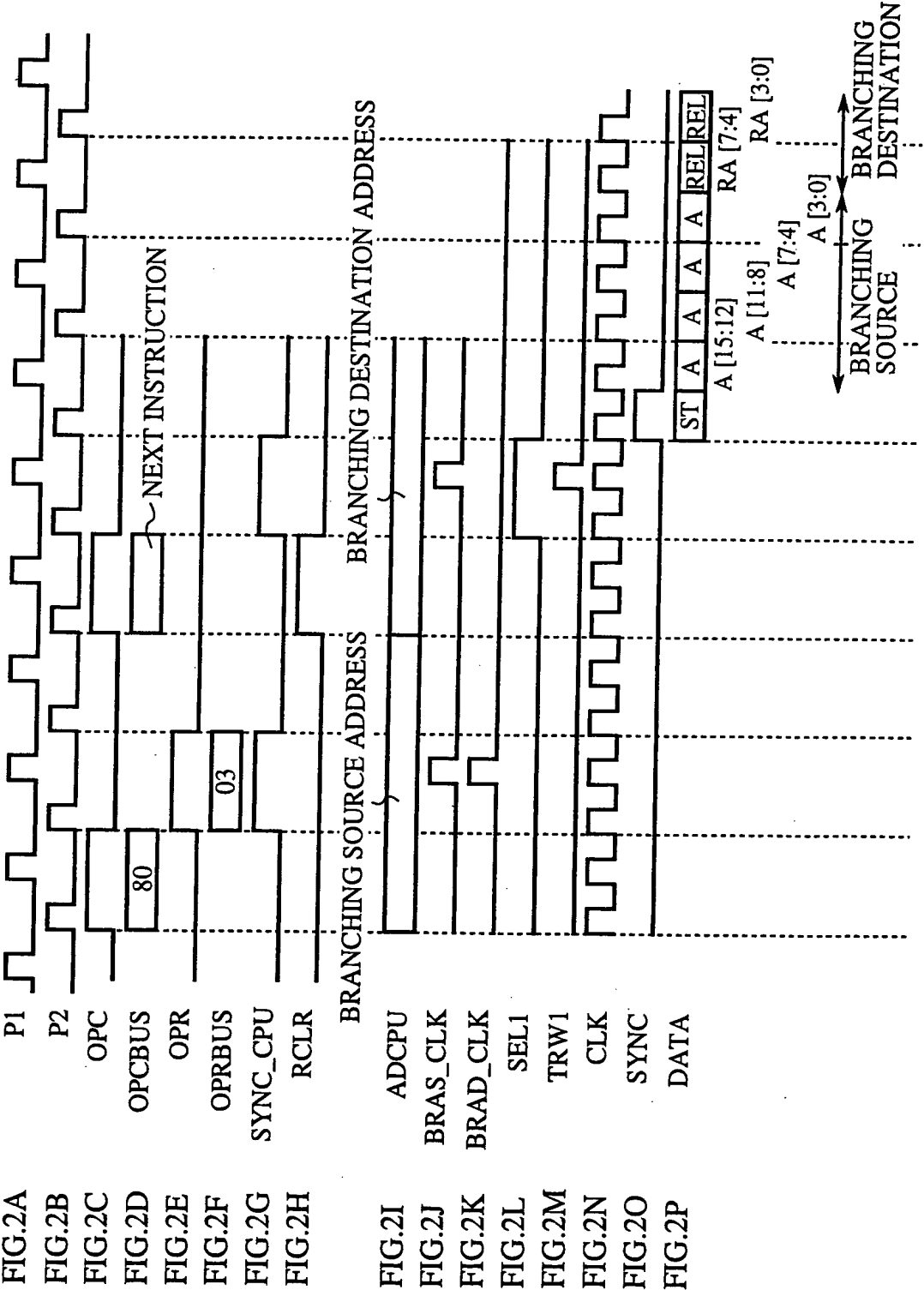
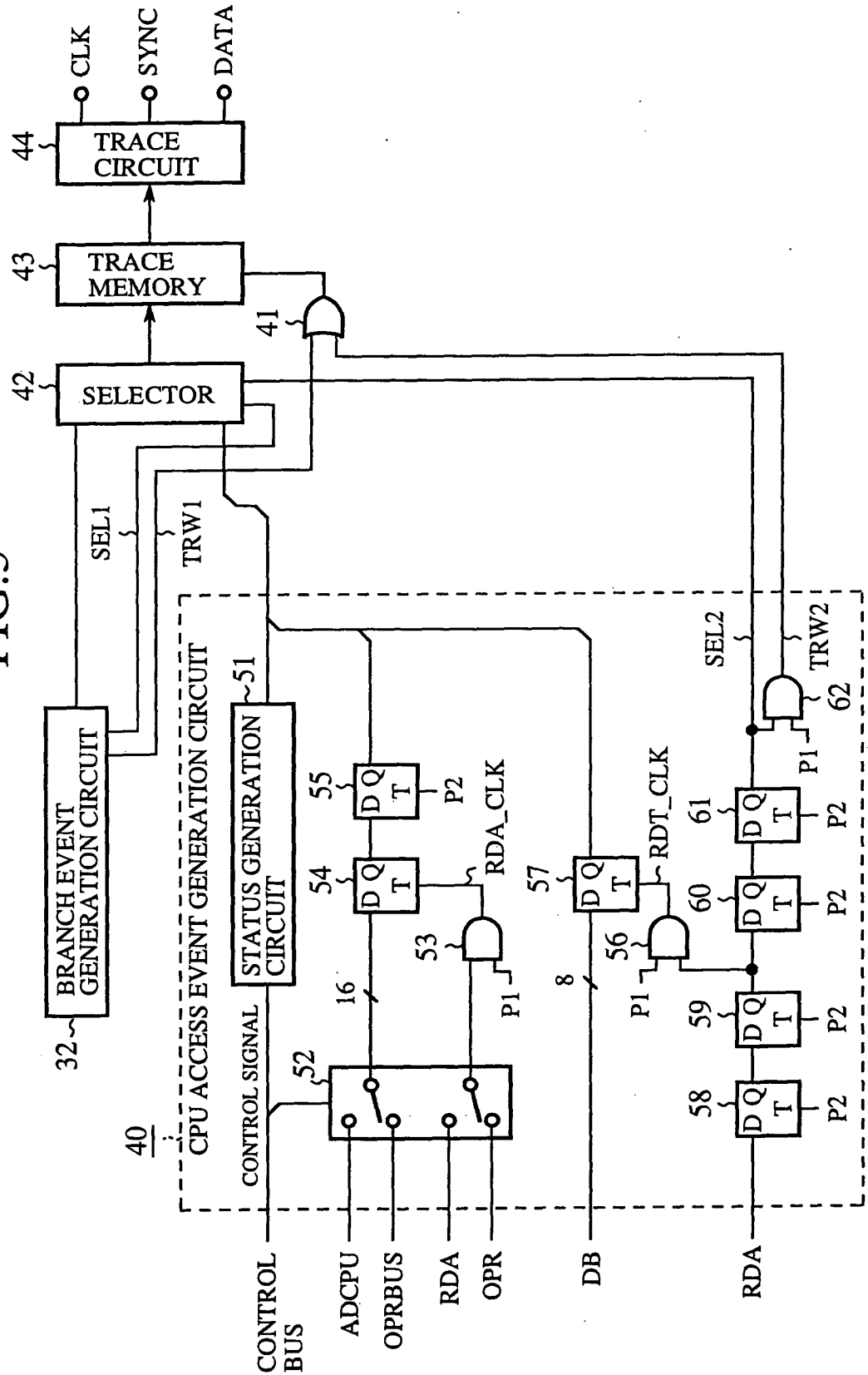


FIG.3



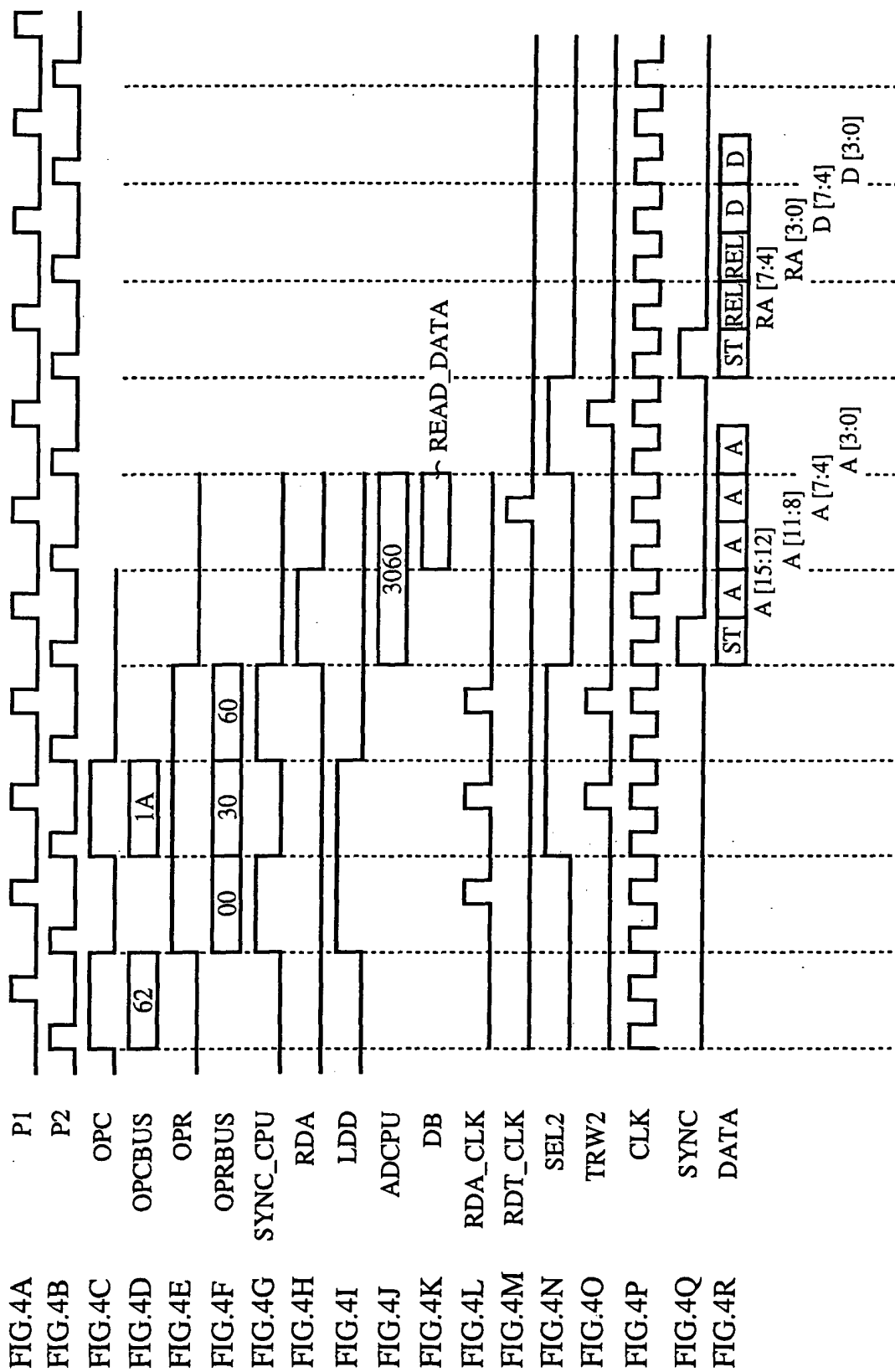
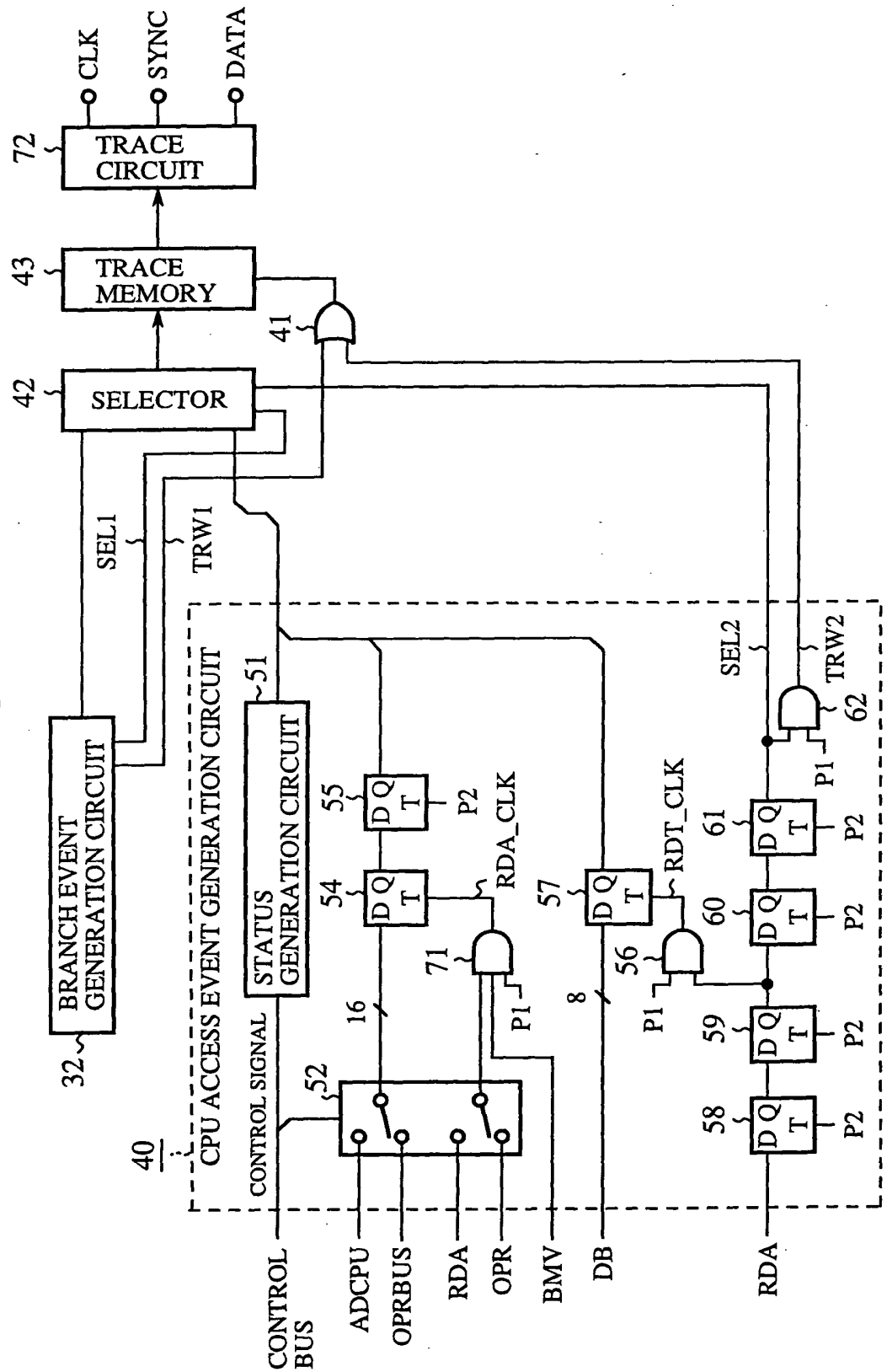


FIG.5



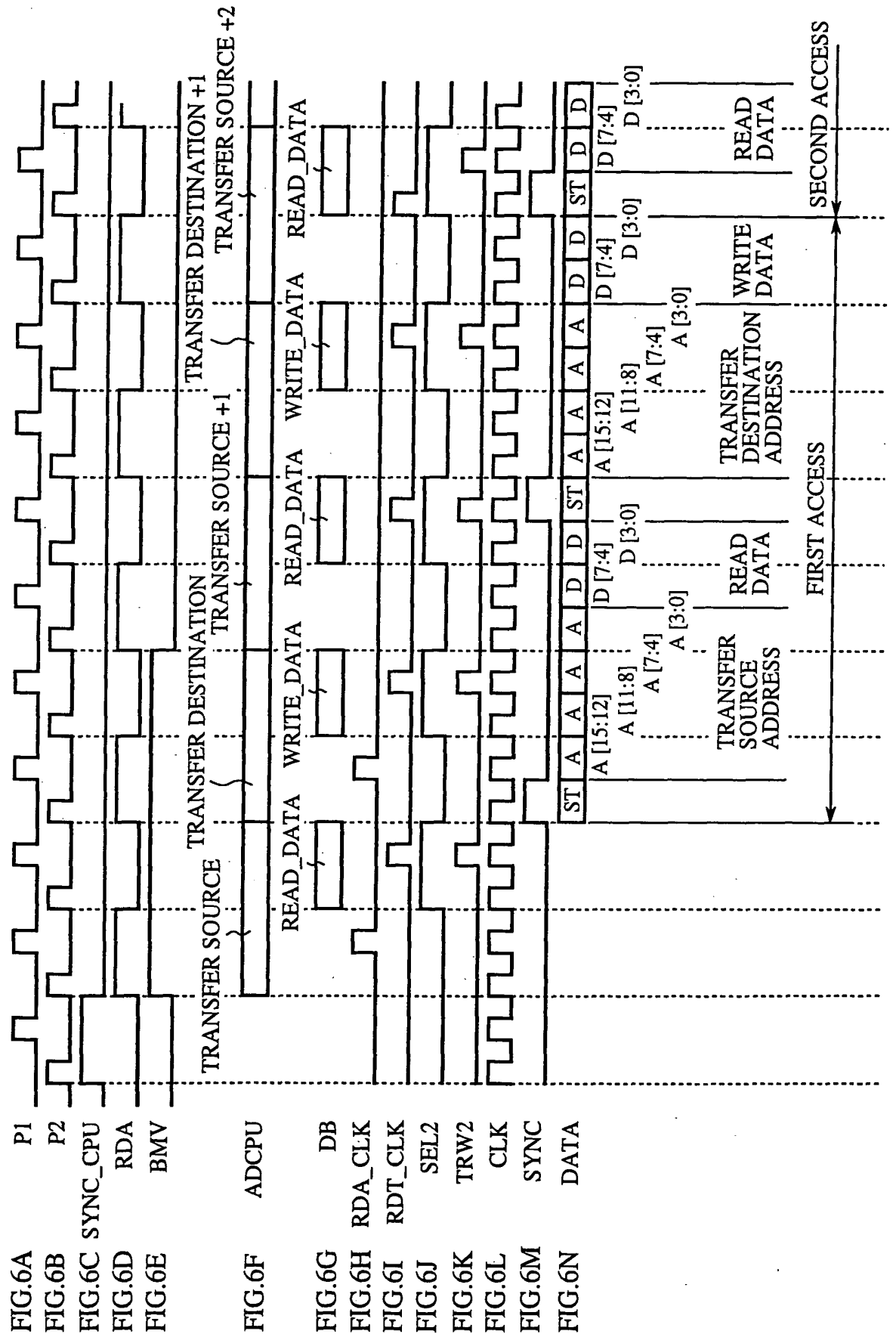


FIG. 7 (PRIOR ART)

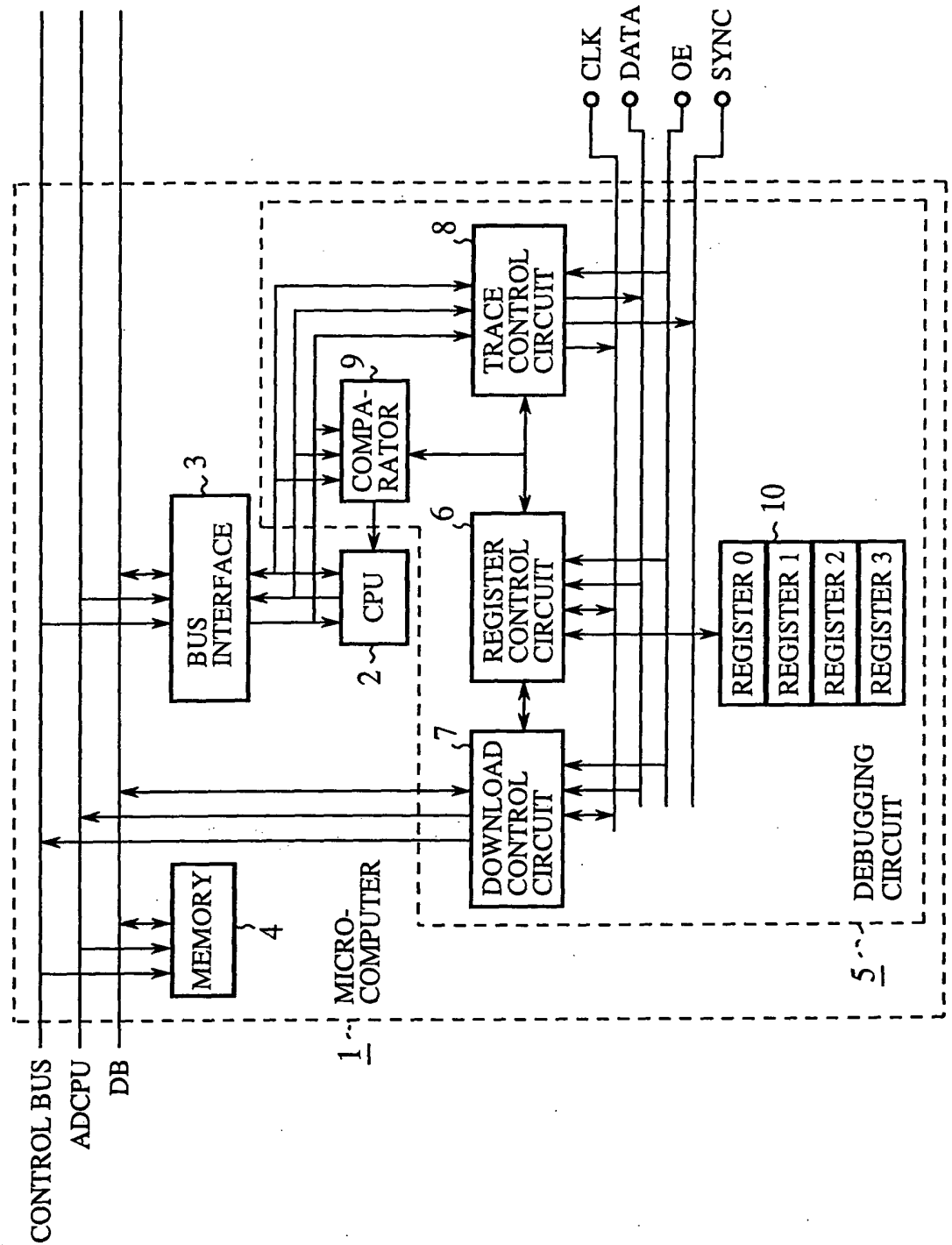
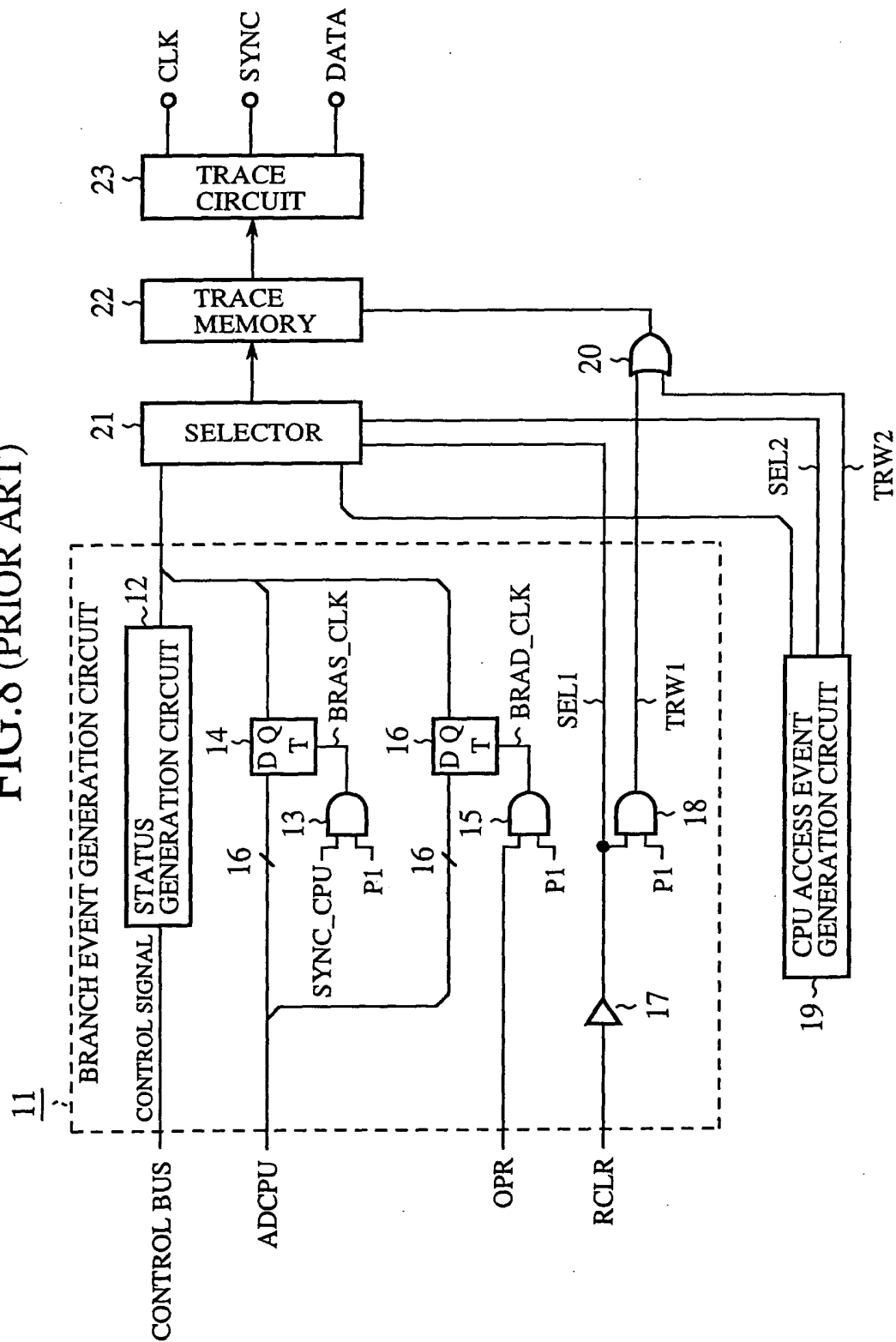


FIG. 8 (PRIOR ART)





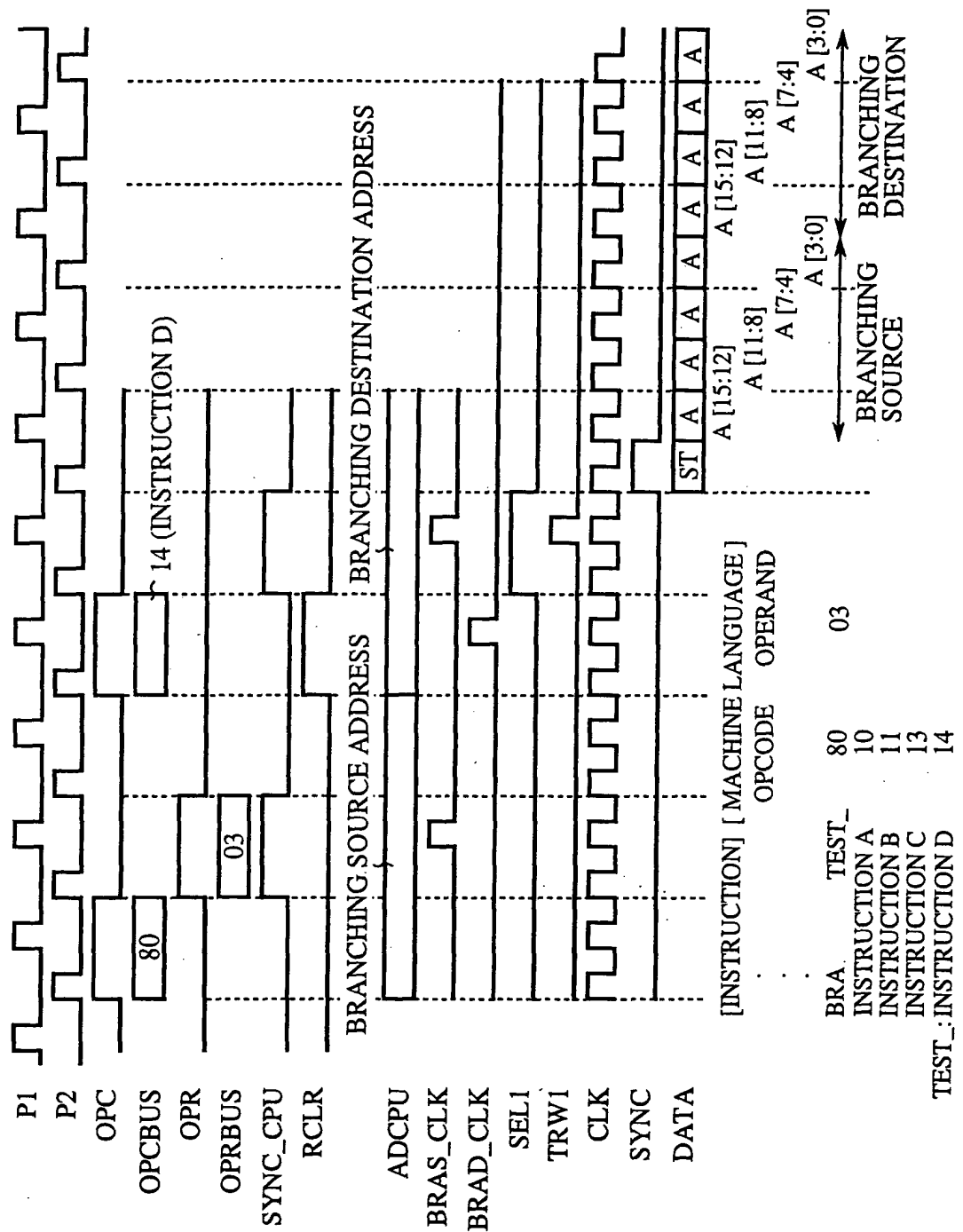
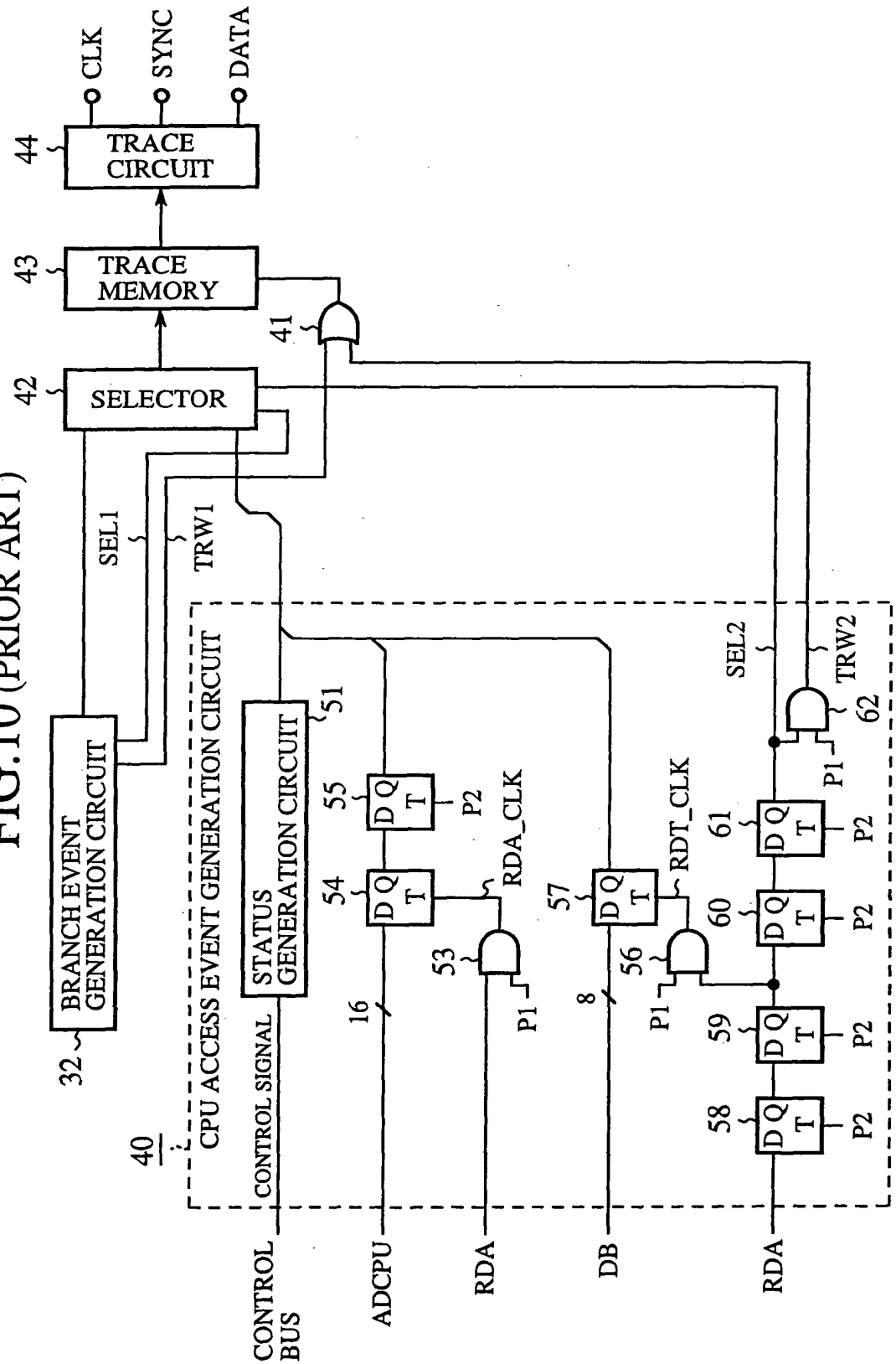


FIG.10 (PRIOR ART)



The timing diagram illustrates the sequence of events for the LDD and LDA instructions. The signals shown are P1, P2, OPC, OPCBUS, OPR, OPRBUS, SYNC\_CPU, RDA, ADCPU, DB, RDA\_CLK, RDT\_CLK, SEL2, TRW2, CLK, SYNC, and DATA. The data bus (DATA) shows the instruction bytes (80, 1A, 00, 03) and the operand (00, 60). The diagram also shows the internal state of the processor, including the program counter (PC) and the instruction register (IR).

# PRIOR ART

